

IN THE CLAIMS

Rewrite the pending elected claims as follows:

1. (Currently amended) A memory system comprising:
at least one channel;
a plurality of memory devices coupled to at least the one channel; and [[,]]
~~wherein the plurality of memory devices includes at least a first memory device~~
~~having a first bandwidth and the first bandwidth is less than a first data block size divided by~~
~~a first time period; and~~
a memory controller coupled to at least the one channel,
wherein ~~during one mode of operation~~ the memory controller provides ~~control~~
~~information~~ a command to at least a first group of memory devices in the plurality of
memory devices via at least the one channel, ~~the first group of memory devices including the~~
~~first memory device, and at least the first group of memory devices, as a multiplexed group,~~
communicate a first data block to the memory controller via at least the one channel during
[[the]] a first time period in accordance with the command; and control information
wherein during the first time period each memory device in the first plurality of
memory devices has a second transfer rate that is less than a first transfer rate for transferring
the first data block during the first time period; and
wherein each one of the memory devices in the first group of memory devices is
configured to communicate in response to the command a respective second data block,
which has a size less than the first data block size, during the first time period.
2. (Cancelled)
3. (Previously presented) The memory system of claim [[2]] 1, including two channels,
each one of the two channels coupled to a second group of memory devices in the plurality of
memory devices to the memory controller.
4. (Currently amended) The memory system of claim ~~3~~ wherein the second group of
memory devices comprises sixteen memory devices 1, wherein a first memory device in the
first group of memory devices is configured to transfer its respective second data block
during a first portion of a first clock cycle of the first time period and a second memory
device in the first group of memory devices is configured to transfer its respective second
data block during a second portion of the first clock cycle of the first time period.

5. (Currently amended) The memory system of claim ~~[[2]]~~ 1, including four full channels and one half channel, each one of the full channels coupled to a first number ~~second group~~ of memory devices in the plurality of memory devices, and the one half channel coupled to half of the first number ~~second group~~ of memory devices.
6. (Currently amended) The memory system of claim 5, wherein the first number ~~second group~~ of memory devices comprises sixteen memory devices.
7. (Currently amended) The memory system of claim ~~[[2]]~~ 1, including eight channels, each of the eight channels coupled to a respective ~~second~~ group of memory devices in the plurality of memory devices.
8. (Currently amended) The memory system of claim 7, wherein the respective ~~second~~ group of memory devices comprises eight memory devices.
9. (Currently amended) The memory system of claim ~~[[2]]~~ 1, including four channels, each of the four channels coupled to a respective ~~second~~ group of memory devices in the plurality of memory devices.
10. (Currently amended) The memory system of claim 9, wherein the respective ~~second~~ group of memory devices comprises eight memory devices.
11. (Currently amended) A memory system comprising:
 - a main channel;
 - at least one repeater coupled to the main channel;
 - at least one auxiliary channel coupled to at least the one repeater;
 - a first plurality of memory devices coupled to at least the one auxiliary channel; and~~[[,]]~~
 - ~~wherein each one of the first plurality of memory devices has a bandwidth that is less than a first data block size divided by a first time period; and~~
 - a memory controller coupled to the main channel,
 wherein during one mode of operation the memory controller provides a command ~~control information~~ to the first plurality of memory devices via the main channel, at least the one repeater and at least the one auxiliary channel, and ~~at least~~ the first plurality of memory devices, as a multiplexed group, communicate a first data block to the memory controller during ~~[[the]]~~ a first time period in accordance with the ~~control information~~ command;

wherein during the first time period each memory device in the first plurality of memory devices has a transfer rate that is less than a transfer rate for transferring the first data block during the first time period; and

wherein each memory device in the first plurality of memory devices communicates in response to the command a respective second data block, which has a size less than the first data block size, during the first time period.

12. (Cancelled).

13. (Currently amended) The memory system of claim 11, including a first auxiliary channel and a second auxiliary channel and a first repeater and a second repeater, and wherein ~~at least the one repeater is coupled to a second~~ the first repeater is coupled to the first plurality of memory devices via the first auxiliary channel, and the second repeater is coupled to a third second plurality of memory devices via the second auxiliary channel.

14. (Currently amended) The memory system of claim 13, wherein the ~~second plurality of memory devices and the third plurality of memory devices each comprise eight memory devices~~ the first repeater is coupled to the second repeater by the main channel.

15. (Withdrawn) A memory system capable of selectively operating in first and second modes, comprising:

a memory controller, memory devices, and a channel connecting the memory controller with the memory devices;

wherein each one of the memory devices is capable of operating in at least a first and a second power state, the first power state consuming more power than the second power state; such that

while the memory system is operating in the first mode, the memory controller is configured to generate a first power down device identification (ID) unique to one of the memory devices, whereby the one memory device upon receiving the first power down device ID will transition from the first power state to the second power state; and

while the memory system is operating in the second mode, the memory controller generates a second power down device ID having the same structure as the first power down device ID, such that a plurality of memory devices upon receiving the second power down device ID transition from the first power state to a second power state.

16. (Withdrawn) A method of reading data in a memory system during a first time period, the memory system comprising a memory controller connected to memory devices via a data bus having multiple data bus lines, the method comprising:

communicating at least one command packet from the memory controller to a plurality of the memory devices;

for each memory device in the plurality of memory devices, seizing at least one data bus line during the first time period and returning data to the memory controller via the at least one data bus line in response to the at least one command packet.

17. (Withdrawn) The method of claim 16, wherein the first time period comprises a sequence of second time periods, and wherein each memory device in the plurality of memory devices seizes at least one data bus line during each one of the second time period.

18. (Withdrawn) The method of claim 17, wherein the data bus implements a wired OR function.

19. (New) The memory system of claim 12, wherein a first memory device in the first group of memory devices is configured to transfer its respective second data block during a first portion of a first clock cycle of the first time period and a second memory device in the first group of memory devices is configured to transfer its respective second data block during a second portion of the first clock cycle of the first time period.